Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1-44. (cancelled)

45. (new) A process for producing a semiconductor device, comprising:

providing a wafer for forming an integrated circuit thereon, the wafer having a main surface on which an integrated circuit is to be formed, a substantially circular contour portion surrounding said main surface, a curved positioning notch formed in said circular contour portion and connecting portions defined between said circular contour portion and said curved positioning notch;

wherein an outer peripheral part of said wafer is chamfered in a thickness direction by mechanical chamfering, and

wherein said connecting portions are chamfered in a plane parallel to said main surface by mechanical chamfering.

46. (new) A process for producing a semiconductor device, comprising:

providing wafer for forming an integrated circuit thereon, the wafer having a main surface on which an integrated circuit is to be formed, a substantially circular contour portion surrounding said main surface, a curved

positioning notch formed in said circular contour portion and connecting portions defined between said circular contour portion and said curved positioning notch;

wherein an outer peripheral part of said wafer is chamfered in a thickness direction by grindstone, and

wherein said connecting portions are chamfered in a plane parallel to said main surface by grindstone.

47. (new) A process for producing a semiconductor device, comprising:

providing a wafer for forming an integrated circuit thereon, the wafer having a main surface on which an integrated circuit is to be formed, a substantially circular contour portion surrounding said main surface, a curved positioning notch formed in said circular contour portion and connecting portions defined between said circular portion and said curved positioning notch, wherein said connecting portions are chamfered in a plane parallel to said main surface; and

positioning said wafer by rotating said wafer.

48. (new) A process for producing a semiconductor device according to claim 47, wherein, in the positioning step, positioning said wafer by using photoelectric elements.

49. (new) A process for producing a semiconductor device according to claim 48, wherein an outer peripheral part of said wafer is chamfered in a thickness direction by mechanical chamfering, and

wherein said connecting portions are chamfered in a plane parallel to said main surface by mechanical chamfering.

50. (new) A process for producing a semiconductor device according to claim 48, wherein an outer peripheral part of said wafer is chamfered in a thickness direction by grindstone, and

wherein said connecting portions are chamfered in a plane parallel to said main surface by grindstone.

51. (new) A process for producing a semiconductor device according to claim 47, wherein, in the positioning step, positioning said wafer by optical means.

52. (new) A process for producing a semiconductor device according to claim 47, wherein an outer peripheral part of said wafer is chamfered in a thickness direction by mechanical chamfering, and

wherein said connecting portions are chamfered in a plane parallel to said main surface by mechanical chamfering.

53. (new) A process for producing a semiconductor device according to claim 47, wherein an outer peripheral part of said wafer is chamfered in a thickness direction by grindstone, and

wherein said connecting portions are chamfered in a plane parallel to said main surface by grindstone.

54. (new) A wafer for forming an integrated circuit thereon, the wafer comprising:

a main surface on which an integrated circuit is to be formed;

a substantially circular contour portion surrounding said main surface;

a curved notch formed in said circular contour portion; and

connecting portions defined between said circular contour portion and said curved notch, wherein said connecting portions are chamfered in a plane parallel to said main surface, and

wherein positioning said wafer by rotating said wafer is to be performed.

55. (new) A wafer for forming an integrated circuit according to claim 54, wherein positioning said wafer by using photoelectric elements is to be performed.

56. (new) A wafer for forming an integrated circuit according to claim 55, wherein an outer peripheral part of said wafer is chamfered in a thickness direction by mechanical chamfering, and

wherein said connecting portions are chamfered in a plane parallel to said main surface by mechanical chamfering.

57. (new) A wafer for forming an integrated circuit according to claim 55, wherein an outer peripheral part of said wafer is chamfered in a thickness direction by grindstone, and

wherein said connecting portions are chamfered in a plane parallel to said main surface by grindstone.

58. (new) A wafer for forming an integrated circuit according to claim 54, wherein positioning wafer by optical means is to be performed.

59. (new) A wafer for forming an integrated circuit according to claim 54, wherein an outer peripheral part of said wafer is chamfered in a thickness direction by mechanical chamfering, and

wherein said connecting portions are chamfered in a plane parallel to said main surface by mechanical chamfering.

60. (new) A wafer for forming an integrated circuit according to claim 54, wherein an outer peripheral part of said wafer is chamfered in a thickness direction by grindstone, and

wherein said connecting portions are chamfered in a plane parallel to said main surface by grindstone.